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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,403	03/12/2004	Shinichi Yoshioka	250327US2S	6014

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EXAMINER	
FLORES, LEON	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/24/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/798,403	YOSHIOKA, SHINICHI	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims (1-3, 6-7, 12-13, 16-20) are rejected under 35 U.S.C. 102(e) as being anticipated by Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1).

Re claim 1, Agrawal discloses a semiconductor integrated circuit device comprising: a first receiver including a first clock data recovery circuit capable of

receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated (See fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44.); a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the first clock data recovery circuit (See fig. 2: 202: TX + Serializer, col. 4, lines 31-36); a second receiver including a second clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated (See fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44.); and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the second clock data recovery circuit. (See fig. 2: 206: TX + Serializer, col. 4, lines 31-36)

Re claim 2, the reference of Agrawal further disclose that wherein the first and second transmitters are arranged between the first and second receivers, and the first and second transmitters are adjacent to the first and second receivers, respectively. (See fig. 2. Furthermore, one skilled in the art would know that the element 204 can be placed either on top/bottom of both SERDERS "202 & 206" within the same chip. It is simply knowing how to route the wires when designing the PCB Board.)

Re claim 3, the reference of Agrawal further disclose that wherein the first and second receivers are arranged between the first and second transmitters, and the first

and second receivers are adjacent to the first and second transmitters, respectively. (See fig. 17. Furthermore, one skilled in the art would know that the element 204 can be placed either on top/bottom of both SERDERS "202 & 206" within the same chip. It is simply knowing how to route the wires when designing the PCB Board.)

Claim 6 has been analyzed and rejected w/r to claim 2 above

Claim 7 has been analyzed and rejected w/r to claim 3 above.

Re claim 12, the reference of Agrawal further disclose that a semiconductor integrated circuit device comprising: a first receiver including a first clock data recovery circuit capable of receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or first phase control information for controlling a phase of a clock (See fig. 2: 202, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44. Furthermore, one skilled in the art would know that this is the way a CDR operate.), and a first deserializer which converts serial data synchronized with the generated clock into parallel data (See fig. 2: 202 ; RCVR + De-serializer CDR "with DPLL") a first transmitter including a first serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the first clock data recovery circuit (See fig. 2: 202: TX + Serializer, col. 4, lines 31-36); a second receiver including a second clock data recovery circuit capable of

receiving serial data, recovering a clock from the received serial data, and changing a phase of a clock to be generated on the basis of a frequency offset between the received serial data and a reference clock, or second phase control information for controlling a phase of a clock, and a second deserializer which converts serial data synchronized with the generated clock into parallel data (See fig. 2: 206, RCVR + De-serializer CDR "with DPLL", col. 4, lines 42-44. Furthermore, one skilled in the art would know that this is the way a CDR operate.); and a second transmitter including a second serializer which converts parallel data into serial data synchronized with one of a transmit clock and the clock generated by the second clock data recovery circuit. (See fig. 2: 206: TX + Serializer, col. 4, lines 31-36)

Re claim 13, the reference of Agrawal further discloses when the second receiver is to be tested, the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information, the first transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery circuit, and the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data, and when the first receiver is to be tested, the second clock data recovery circuit changes a phase of a clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter, the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock

output from the second clock data recovery circuit, and the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data. (The steps performed in this claim are inherent when testing these chips.)

Claim 16 has been analyzed and rejected w/r to claim 2 above.

Claim 17 has been analyzed and rejected w/r to claim 3 above.

Claim 18 has been analyzed and rejected w/r to claim 2 above.

Claim 19 has been analyzed and rejected w/r to claim 3 above.

Claim 20 is a method claim corresponding to system claim 1 and 12. Hence, the elements in system claims 1 & 12 would have necessitated the steps performed in method claim 20. Therefore, claim 20 has been analyzed and rejected w/r to claims 1 and 12 above.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims (4-5, 8-11 & 13-14) are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1), as applied to claim 1, in view of Evans (US Publication 2003/0196139 A1).**

Re claim 4, the reference of Agrawal fails to specifically disclose a first loop-back path which loops serial data from the first transmitter back to the second receiver; and a second loop-back path which loops serial data from the second transmitter back to the first receiver, wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip.

However, Evans does. (See fig. 17B & paragraph 92) Evans discloses a first loop-back path which loops serial data from the first transmitter (0) back to the second receiver (1); and a second loop-back path which loops serial data from the second transmitter (1) back to the first receiver (0), wherein the first and second loop-back paths are formed in a semiconductor integrated circuit device chip. (See fig. 16B)

Therefore, taking the combined teachings of Agrawal and Evans as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated this step

into the system of Agrawal in the manner as claimed, and as taught by Evans, for the benefit of implementing automated self testing operations. (See paragraph 91)

Claim 5 has been analyzed and rejected w/r to claim 4 above.

Re claim 8, the combination of Agrawal and Evans further discloses a third loop-back path which loops serial data from the first transmitter back to the first receiver (See fig. 17A: element 0, and paragraph 92); and a fourth loop-back path which loops serial data from the second transmitter back to the second receiver (See fig. 17A: element 1, and paragraph 92), wherein the third and fourth loop-back paths are formed in the semiconductor integrated circuit device chip. (See fig. 16B)

Claim 9 has been analyzed and rejected w/r to claim 8 above.

Claim 10 has been analyzed and rejected w/r to claim 8 above.

Claim 11 has been analyzed and rejected w/r to claim 8 above.

Re claim 13, the combination of Agrawal and Evans further discloses when the second receiver is to be tested, the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information (In Agrawal, see fig. 2: 202), and outputs the phase-changed clock to the first transmitter; the first

transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery circuit (In Evans, see fig. 18A: elements 1 & 2. Furthermore, Rx in element 1 transmit to Tx in element 1), and the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data (In Evans, see fig. 18A: Rx in element 2 receives a signal from element Tx in element 1), and when the first receiver is to be tested, the second clock data recovery circuit changes a phase of a clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter, the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock output from the second clock data recovery circuit (In Evans, see fig. 19A: elements 6 & 7. Furthermore, Rx in element 7 transmit to Tx in element 7), and the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data. (In Evans, see fig. 19A: Rx in element 6 receives a signal from element Tx in element 7. Furthermore, Evans teaches how chips are constantly communicating with each other when operating in a test mode. But, Evans does not disclose that each core "transceiver" has a CDR. However, Agrawal does. Thus, making this combination of references suitable for rejecting claim 13.)

Re claim 14, the combination of Agrawal and Evans further discloses a test control pattern generator (See fig. 2: REFCLK <0:3> from clock tree); and a test

analyzer (See fig. 2: element 204 has a phase comparator. Furthermore, each receiver may employ its own DPLL), wherein the test control pattern generator generates the first and second phase control information (See fig. 2: the REFCLK is inputted to each SERDES), and the test analyzer analyzes a state of the second clock data recovery circuit on the basis of the first phase control information and phase information of the clock recovered by the second clock data recovery circuit, and analyzes a state of the first clock data recovery circuit on the basis of the second phase control information and phase information of the clock recovered by the first clock data recovery circuit. (See fig. 2 & col. 4, lines 42-44. Each Receiver may employ its own PLL. Furthermore, One skilled in the art would know that each Receiver in elements 202 & 206 operate in the manner as claimed, providing each receiver is in CDR mode.)

Claims (13, 15 & 20) are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (hereinafter Agrawal) (US Patent 7,098,685 B1), as applied to claim 1 & 12, in view of Goldrian (US Patent 5,742,798).

Re claim 15, the reference of Agrawal fails to specifically disclose that wherein the test analyzer comprises a first test analyzing circuit which analyzes the state of the first clock data recovery circuit (See fig. 2: the phase comparator in element 202), and a second test analyzing circuit which analyzes the state of the second clock data recovery circuit. (See fig. 2: the phase comparator in element 206) the test control pattern generator comprises a first test control pattern generating circuit which generates the first phase control information (See fig. 2: REFCLK <0:3> from clock tree). But the

reference of Agrawal fails to specifically disclose a second test control pattern generating circuit which generates the second phase control information.

However, Goldrian does. (See fig. 5: 515 & col. 4, lines 48-51). Goldrian discloses a second test control pattern generating circuit which generates the second phase control information. Furthermore, each of the chips A & B contain a variable clock delay which adjusts the variable clock delay on each chip, allowing to synchronize chip clock A and B with respect to each other.

Therefore, taking the combined teachings of Agrawal and Goldrian as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Agrawal in the manner as claimed, and as taught by Goldrian, for the benefit of facilitating an optimization of the data transfer rate. (See col. 3, lines 25-26)

Re claim 13, the combination of Agrawal and Goldrian further discloses when the second receiver is to be tested (In Goldrian, when testing one of the chips), the first clock data recovery circuit changes a phase of a clock to be generated on the basis of the first phase control information (In Goldrian, see fig. 7B & col. 6, lines 27-56. Furthermore, Once the comparison has been made, if the comparison is not fulfilled delay A will be further incremented until chip A and B are synchronized.), and outputs the phase-changed clock to the first transmitter (In Goldrian, see col. 3, lines 48-54. There is a feedback line which connects the driver module to the variable clock delay.), the first transmitter transmits, to the second clock data recovery circuit, serial data synchronized with the phase-changed clock output from the first clock data recovery

circuit (In Goldrian, see fig. 2 & col. 51-56), and the second clock data recovery circuit receives the serial data transmitted from the first transmitter, and recovers the clock from the received serial data (In Goldrian, Chip B receives the data. Furthermore, Goldrian teaches how two chips, having two different clocks, constantly communicating with each other, can achieve synchronization. But, Goldrian does not achieve synchronization by means of CDRs. However, Agrawal does. Thus, making this combination of references suitable for rejecting claim 13.), and when the first receiver is to be tested, the second clock data recovery circuit changes a phase of a clock to be generated on the basis of the second phase control information, and outputs the phase-changed clock to the second transmitter, the second transmitter transmits, to the first clock data recovery circuit, serial data synchronized with the phase-changed clock output from the second clock data recovery circuit, and the first clock data recovery circuit receives the serial data transmitted from the second transmitter, and recovers the clock from the received serial data. (And vice versa, meaning, when testing the other chip.)

Claim 20 has been analyzed and rejected w/r to claim 12, 13, and 14.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,650,141 B2 by Agrawal et al discloses a high speed interface for a programmable interconnect circuit.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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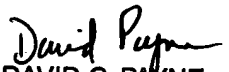
March 30, 2007



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